

**STATE UNIVERSITY OF NEW YORK COLLEGE AT NEW PALTZ
DIVISION OF ENGINEERING PROGRAMS**

**EGC221-03 Digital Logic Lab – 1 Credit
Fall 2017 Semester**

Instructor: Dr. Damu Radhakrishnan, 204 Resnick Engineering Hall
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Lab Session: Friday 8.00 -10.45 WH221
Office Hours: Thursday 11.00 – 12:30pm

Corequisites: EGC220 Digital Logic Fundamentals

Course catalog description: Experiments in both combinational and sequential logic design. Breadboarding, schematic capture, and Verilog implementation of digital circuits of varying complexity. Use of software tools such as Altera Quartus II to design FPGA based circuits.

Course learning outcomes:

- I. Students will learn to analyze, design, simulate, and build combinational logic and clocked sequential circuits using modern computer engineering tools and techniques.
- II. Students will enhance their technical writing skills through a series of formal lab reports that increase in complexity as the semester progresses.

This course contributes to the student outcomes as specified in the following table:

Student Outcome	Learning Outcome	Level of Contribution 3 /3 = strong; 2/3 = moderate; 1/3 = marginal
a) An ability to apply knowledge of mathematics, science and engineering	I	3/3
d) An ability to function on multidisciplinary teams.	II	3/3

Textbook: No textbook is required for this course.

References:

- ◆ “*Digital Design*”, 5th Edition, Mano/Ciletti, Prentice Hall, Upper Saddle River, NJ , 2013, ISBN 978-0-13-277420-8
- ◆ "*Logic and Computer Design Fundamentals*," 4th Edition, by M. Mano and C. Kime, Prentice Hall, Upper Saddle River, NJ, 2008
- ◆ "*Fundamentals of Logic Design*", by C. H. Roth, Jr, PWS Publishing Company.

- ◆ *"Digital Design and Computer Architecture,"* David Money Harris and Sarah Harris, Morgan Kaufmann Publ, 2007
- ◆ *"Digital Design"* 3rd Edition by J. F. Wakerly, Prentice Hall, Upper Saddle River, NJ, 2000.
- ◆ *"Digital Principles,"* 3rd Ed, Roger L. Tokheim, Schaum's Outline Series, McGraw-Hill Publ, 1994 [contains many worked out examples]
- ◆ *"Introduction to Digital Systems",* by Palmer and Perlman, Schaum's Outline Series, McGraw-Hill, New York, 1993 [contains many worked out examples].

Assignments:

Assignments will be posted on blackboard.

The students should review the lab prior to the scheduled lab period and be prepared for the lab. A brief overview of the lab experiment will be given at the beginning of each new lab session.

Tentative lab schedules are as follows:

LABS:

Lab 1 – **Basic Logic Gate Simulation**

Lab 2 – **Basic Logic Gate Physical Verification**

Lab 3 – **Combinational Logic Circuits**

Lab 4 – **Combinational Logic Circuit Reduction**

Lab 5 – **Arithmetic Circuits Using Altera Quartus II**

Lab 6 – **Hierarchical Logic Circuits Using Altera Quartus II**

Lab 7 – **Arithmetic Logic Unit (ALU) Schematic Implementation**

Lab 8 – **Arithmetic Logic Unit (ALU) Verilog Implementation**

Lab 9 – **Sequential Design using Verilog**

Design Team:

Teams of two students will complete each lab as a unit. Keep a notebook for the lab.

Write all background preparation in your notebook. Team members must be active in all phases of the lab. Inactive team member can be removed at the discretion of other team member or the instructor. Inactivity of team members should be brought to the attention of the instructor. Each team is to turn in one lab report at the beginning of the next lab session.

Grading Policy:

Category	Weights
End of semester presentation	10%
Lab reports:	75%
Attendance and participation	15%
Total:	100%

Each lab report is graded on a 0-10 point scale. A report without a signature is graded on a 0-5 point scale.

Presentation:

Each team is expected to make a Power Point presentation of 10 to 15 minutes on the last day of lab. You may consult with me and choose one of the labs. Your presentation should include your design problem and your solution at the appropriate detail. You should conclude with encountered problems and lessons learned.

Relevant Web Sites:

- ◆ Digital Logic Fundamentals: http://www.williamson-labs.com/480_logic.htm
- ◆ Digital logic tutorial: <http://www.play-hookey.com/digital/>
- ◆ Combinational Logic Tutorial:
<http://www.ee.surrey.ac.uk/Projects/Labview/combindex.html>
- ◆ Latches and Flip flops:
<http://vorlon.cwru.edu/~jackie/eces301/hw/HW2/lab2.html>
- ◆ Texas Instruments Digital Logic Families:
<http://focus.ti.com/docs/logic/logichomepage.jhtml>
- ◆ To download a demo version of LogiSim click on
<https://sourceforge.net/projects/circuit/>

Rules and general comments:

- ◆ Attendance policy: I strongly advise against missing any labs. If you miss a lab, it is your responsibility to obtain assignments and other information given on that day. You will not be penalized for the first missed lab. However, each additional missed lab will result in loss of 5% of the overall grade up to a total of 15%.
- ◆ Common courtesy is expected in class. **Please turn off your cell phone or put it on silent mode while in class.**
- ◆ Please make sure you save your graded labs. I may ask for them in case of any grading discrepancy.
- ◆ "I" indicates that the student has done satisfactory work in the course, but because of circumstances beyond his control has been unable to finish all requirements. It is not to be given to enable a student to do additional work to bring up a deficient grade.

Campus-wide Policy Statements

1. Academic integrity policy statement: *Students are expected to maintain the highest standards of honesty in their college work. Cheating, forgery, and plagiarism are serious offenses, and students found guilty of any form of academic dishonesty are subject to disciplinary action. New Paltz's policy on academic integrity is found at http://www.newpaltz.edu/ugc/policies/policies_integrity.html, and several excellent resources to help with avoiding plagiarism are available on the Sojourner Truth Library's website: <http://lib.newpaltz.edu/assistance/plag.html>.*

2. Reasonable accommodation of individuals with disabilities statement: *Students needing classroom and/or testing accommodations related to a disability should contact the Disability Resource Center (Student Union, Room 210, 845-257-3020) as close as possible to the beginning of the semester. The DRC will then provide students' instructors with an Accommodation Memo verifying the need for accommodations. Specific questions about services and accommodations may be directed to Deanna Knapp, Assistant Director (knappd@newpaltz.edu).*

3. Veteran and Military Services statement: *New Paltz's Office of Veteran and Military Services (OVMS) is committed to serving the needs of veterans, service members and their dependents during their transition from military life to student life. Student veterans, service members or their dependents who need assistance while attending SUNY New Paltz may refer to www.newpaltz.edu/veterans; call 845-257-3120, -3124 or -3074; or stop by the Student Union, Room 100 South.*

4. Computer and network policies statement: *Users of New Paltz's computer resources and network facilities are required to comply with the institutional policies outlined in the Acceptable Uses and Privacy Policy (<https://sites.newpaltz.edu/csc/policies/acceptable-uses-and-privacy-policy/>).*

5. Identity verification policy statement for online courses: *New Paltz's Online Identity Verification Policy is designed to verify that students enrolled in our online courses and/or programs are the ones who take the courses, complete the programs, and receive the academic credit. See http://www.newpaltz.edu/ugc/policies/policies_onlineverification.html for the complete policy.*

Information on electronic SEIs

The fall 2017 end-of-semester SEIs will be administered **November 29–December 12**. *I value your feedback and use it to improve my teaching and planning. Please complete the online form during the open period.*

Important dates

Last day to withdraw from a course (undergraduates) without receiving a penalty grade: November 3, 2017.